**What is claim d is:**

1. A single chip Ethernet switch comprising:

a physical layer entity (PHY) including a plurality of ports;

an address table for being written to and read out information to operate the plurality of ports;

a switch for switching the Ethernet switch to a daisy chain test mode; and

an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively.

2. The switch of claim 1, further comprising an input for receiving the test packet.

3. The switch of claim 1, further comprising a packet generator for generating the test packet.

4. The switch of claim 3, further comprising a register for storing information of the test packet.

5. The switch of claim 1, further comprising a

verification unit for verifying the test packet.

6. The switch of claim 1, further comprising an output for sending out the test packet.

7. The switch of claim 1, wherein the test engine includes a writing apparatus for writing a set of initial addresses to the address table under the daisy chain test mode.

8. The switch of claim 1, wherein the packet source address learning process sets a packet destination address as a next port.

9. A daisy chain test for a single chip Ethernet switch integrated with a physical layer entity including a plurality of ports, the switch having an address table for being written to and read out information to operate the plurality of ports, the test comprising the steps of:

connecting each of the plurality of ports to a respective passive loop-back device;

selecting a start transmission port and a stop receiving port from the plurality of ports;

supplying a test packet to the start transmission port; and

proceeding a packet source address learning process for

delivering the test packet from the start transmission port to the stop receiving port progressively.

10. The test of claim 9, further comprising inputting the test packet to the switch.

11. The test of claim 9, further comprising generating the test packet in the switch.

12. The test of claim 9, further comprising verifying the test packet after the stop receiving port.

13. The test of claim 12, further comprising sending out the test packet from the stop receiving port.

14. The test of claim 9, wherein the learning process sets a packet destination address as a next port.